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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,796	03/23/2001	Paul E. McKenney	BEA9-2001-0001-US1	5819
49056	7590	08/11/2005	EXAMINER	
LIEBERMAN & BRANDSDORFER, LLC 12221 MCDONALD CHAPEL DRIVE GAITHERSBURG, MD 20878			TSAI, HENRY	
			ART UNIT	PAPER NUMBER

2183

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/816,796

Applicant(s)

MCKENNEY, PAUL E.

Examiner

Henry W.H. Tsai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Robertson (U.S. Patent No. 5,850,632), hereafter referred to as Robertson'632.

Referring to claims 1 and 12, Robertson'632 discloses as claimed a method for maximizing CPU performance in a multiprocessor (see Fig. 2), comprising:

allowing write operations in local memory (each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is broadly interpreted as a local memory) to execute in an arbitrary order (see col. 16, lines 31-34, regarding the caches being fully associative. Note each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is individually and locally used by the

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associated processors 71-74, see Fig. 2; and a full associative replacement algorithm is used to have an arbitrary order to replace the cache lines thereof) and at any time prior to storing a pointer (PC, program counter) to a new element of a shared resource (Program counter register in the Robertson'632's system) (note PC will be incremented or changed to a new number after the write operation); explicitly indicating a set of write operations to non-local memory (memory configuration cache 305, see Fig. 2, is broadly interpreted as a non-local memory since it is not disposed inside the processors 71-74, see Fig. 2) be conducted in a specified order (see col. 31, lines 38-57, regarding the specified order for writing (replacing) the cache lines of the memory configuration cache 305); and forcing said write operation to non-local memory (memory configuration cache 305, see Fig. 2, is broadly interpreted as a non-local memory since it is not disposed inside the processors 71-74, see Fig. 2) to precede storing said pointer to said new element of said shared resource (note the forcing step occurs when the Robertson'632's system also has a memory access to memory configuration cache 305).

As to claims 2, 13, and 23, Robertson'632 also discloses: assigning first and second registers of a CPU for storing associated first and second instruction addresses (note the

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Robertson'632's processor certainly comprises registers such as PC (program counter), MAR (memory address register), General Data/Address Registers, or CAR (control address register for storing instruction addresses).

As to claim 3, Robertson'632 also discloses: providing a third instruction referencing said registers (this is the situation when the registers, such as PC (program counter), MAR (memory address register), General Data/Address Registers, or CAR (control address register) storing the first and second instruction addresses is referred to as the source or destination registers in a third instruction).

As to claims 4 and 14, Robertson'632 also discloses: said third instruction specifies ordering between said first and second instructions (this is the situation when the registers storing the first and second instruction addresses are referred to as the destination registers in a third LOAD instruction, therefore, certainly operating the ordering between said first and second instructions).

As to claims 5 and 15, Robertson'632 also discloses: said third instruction indicates said first instruction's execution attaining a first specified state of execution prior to said second instruction's execution attaining a second specified state of execution (note this occurs in the Robertson'632's

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system when either one of the first instruction and the second instruction depends from the other and each instruction's execution invokes its state of execution specified by such as its opcode).

As to claims 6 and 16, Robertson'632 also discloses: said first and said second specified states of execution are selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an I/O access, and completing instruction execution (note this occurs in the Robertson'632's system when the first instruction and the second instruction is a memory load/store operation and it therefore certainly involves at least one of initiating memory access, completing a memory access as claimed).

As to claims 7, 17, and 24, Robertson'632 also discloses: assigning a sequence number to an associated instruction for maintaining instruction ordering (note this is the situation in the Robertson'632's system when a sequence of program to be executed is saved in the Robertson'632's main memory and each instruction in the program is assigned by a logical address or physical address number)

As to claims 8 and 18, Robertson'632 also discloses: statically encoding said sequence number within said instruction

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(inherently existing in the Robertson'632's processor when a sequence of program is therein).

As to claims 9 and 19, Robertson'632 also discloses: dynamically encoding said sequence number within said instruction (as set forth above, inherently the Robertson'632's processor comprises registers such as MAR (memory address register), General Data/Address Registers, or CAR (control address register for storing instruction addresses and for dynamically encoding the sequence number).

As to claims 10 and 20, Robertson'632 also discloses: placing a range of instructions into a hierarchical ordering system (note the control unit of the Robertson'632's CPU is reasonably and broadly interpreted as a hierarchical ordering system and a range of instructions is inherently placed in a process table).

As to claims 11, 21 and 25, Robertson'632 also discloses: implementing a special instruction for maintaining a hierarchical execution of said instruction (such as a microinstruction, existing in the Robertson'632's processor for control the instruction execution, which is broadly interpreted as a special instruction for maintaining a hierarchical execution).

Referring to claim 22, Robertson'632 discloses as claimed a

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processor for use in a multiprocessor computer system (see Fig. 2), comprising: a first instruction for allowing write operations in local memory (each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is broadly interpreted as a local memory) to occur in an arbitrary order (see col. 16, lines 31-34, regarding the caches being fully associative. Note each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is individually and locally used by the associated processors 71-74, see Fig. 2; and a full associative replacement algorithm is used to have an arbitrary order to replace the cache lines thereof), a second instruction for explicitly indicating a set of write operations to non-local memory (memory configuration cache 305, see Fig. 2, is broadly interpreted as a non-local memory since it is not inside the processors 71-74, see Fig. 2) to be conducted in a specified order (see col. 31, lines 38-57, regarding the specified order for writing (replacing) the cache lines of the memory configuration cache 305), wherein write operations to non-local memory must execute prior to storage of a pointer (PC, program counter) to a new element of a shared resource (Program counter register in the Robertson'632's system) (note PC will be incremented or changed to a new number after the write operation); and a third instruction for managing order of execution of said first and second instructions (note



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the above limitations are disclosed by Robertson'632 as set forth above in claim 4); wherein execution of said second instruction is responsive to said first instruction reaching a specified state of execution and said specified state of execution is selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an I/O access, and completing instruction execution (note the above limitations are disclosed by Robertson'632 as set forth above in claims 5 and 6).

### ***Response to Amendment***

3. Applicant's arguments filed 5/23/05 have been fully considered but they are not deemed to be persuasive.

Applicants argue that "Robertson does not disclose modifying a shared resource. Nor does Robertson force a write operation to non-local memory to precede the storage of a reference from an existing element of a shared resource to a new element of the shared resource, and allow a write operation to local memory to execute in an arbitrary order, i.e., at any time prior to storing the point from the existing element of the

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shared resource to the new element of the shared resource. (page 7, last three lines and page 8, lines 1-3). Examiner disagrees with Applicants. Note "to precede the storage of a reference from an existing element of a shared resource to a new element of the shared resource" and "at any time prior to storing the point from the existing element of the shared resource to the new element of the shared resource" are not the claimed limitations. As set forth in the art rejections above, Robertson'632 discloses as claimed: allowing write operations in local memory (each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is broadly interpreted as a local memory) to execute in an arbitrary order (see col. 16, lines 31-34, regarding the caches being fully associative. Note each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is individually and locally used by the associated processors 71-74, see Fig. 2; and a full associative replacement algorithm is used to have an arbitrary order to replace the cache lines thereof) and at any time prior to storing a pointer (PC, program counter) to a new element of a shared resource (Program counter register in the Robertson'632's system) (note PC will be incremented or changed to a new number after the write operation).

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Applicants further argue that "there is no teaching in Robertson for allowing an arbitrary order of execution of write operations from local memory while requiring execution of write operations between local and non-local be executed prior to storing a pointer within a new element in a share resource" (page 8, lines 10-12). Examiner disagrees with Applicants. Note "allowing an arbitrary order of execution of write operations from local memory while requiring execution of write operations between local and non-local be executed prior to storing a pointer within a new element in a share resource" is not the claimed limitations. The argument is moot. As set forth in the art rejections above, Robertson'632 discloses as claimed: allowing write operations in local memory (each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is broadly interpreted as a local memory) to execute in an arbitrary order (see col. 16, lines 31-34, regarding the caches being fully associative. Note each of the instruction caches 21, 26, 31, and 36, see Fig. 2, is individually and locally used by the associated processors 71-74, see Fig. 2; and a full associative replacement algorithm is used to have an arbitrary order to replace the cache lines thereof) and at any time prior to storing a pointer (PC, program counter) to a new element of a shared resource (Program counter register in the Robertson'632's

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system) (note PC will be incremented or changed to a new number after the write operation); explicitly indicating a set of write operations to non-local memory (memory configuration cache 305, see Fig. 2, is broadly interpreted as a non-local memory since it is not disposed inside the processors 71-74, see Fig. 2) be conducted in a specified order (see col. 31, lines 38-57, regarding the specified order for writing (replacing) the cache lines of the memory configuration cache 305).

Applicants further argue that "Robertson does not support the element of forcing a write operation to non-local memory to precede storage of a reference from an existing element of a shared resource to a new element of the shared resource" (page 8, lines 19-21). Examiner disagrees with Applicants. Again, "forcing a write operation to non-local memory to precede storage of a reference from an existing element of a shared resource to a new element of the shared resource" is not the claimed limitation. As set forth in the art rejection, Robertson'632 discloses, as claimed, forcing said write operation to non-local memory (memory configuration cache 305, see Fig. 2, is broadly interpreted as a non-local memory since it is not disposed inside the processors 71-74, see Fig. 2) to precede storing said pointer to said new element of said shared resource (note the forcing step occurs when the Robertson'632's

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system also has a memory access to memory configuration cache  
305).

In summary, Robertson'632 teaches the claimed invention.

#### **Conclusion**

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

#### **Contact Information**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry

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Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, 571-272-2100.

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number: 571-273-8300. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI  
PRIMARY EXAMINER

August 5, 2005